CLAIMS

We claim:

1. An apparatus comprising:

credit management logic to communicate to a chipset an available amount of memory credits in an input/output (I/O) controller;

a first buffer of a first memory size contained within the I/O controller coupled to, and in communication with the credit management logic; and

a second buffer of a second memory size contained within the I/O controller coupled to, and in communication with the credit management logic.

2. The apparatus of claim 1, wherein the first buffer and the second buffer are the same size.

3. The apparatus of claim 2, wherein the first buffer and the second buffer are about 64 bytes to about 64 kilobytes in size.

4. The apparatus of claim 1, wherein the first buffer and the second buffer are different sizes.

5. The apparatus of claim 4, wherein the first buffer and the second buffer are about 64 bytes to about 64 kilobytes in size.

6. The apparatus of claim 1, further comprising:

a transaction layer containing the credit management logic; and

an internal switch to divide data received from the chipset between one of the first buffer, the second buffer and both the first and second buffers.

7. The apparatus of claim 1, wherein the I/O controller is one of a bridge, a switch, an endpoint and a root complex.

8. A method comprising:

determining an amount of available memory credits in an input/output (I/O) controller;

communicating to a chipset coupled to the I/O controller the amount of available memory credits; and

sending an amount of data from the chipset to the I/O controller, the amount of data sent being one of equivalent to and less than the communicated available memory credit amount.

9. The method of claim 8, wherein determining the available amount of memory credits comprises:

comparing an amount of available memory in each of a plurality of buffers contained within the I/O controller; and

determining a least amount of available memory in one of the plurality of buffers to create an amount of available memory in the I/O controller.

10. The method of claim 9, further comprising:

converting the amount of available memory in the I/O controller to an amount of available memory credits.

11. The method of claim 10, wherein converting the amount of available memory to an amount of available memory credits comprises:

dividing the available amount of memory in the I/O controller by an amount of memory equivalent to one credit.

12. The method of claim 9, further comprising:

temporarily storing the data sent from the chipset in the I/O controller.

13. The method of claim 12, wherein temporarily storing the data comprises:

temporarily storing the data in at least one buffer contained within the I/O controller.

14. The method of claim 13, wherein temporarily storing the data in at least one buffer comprises:

storing the data in a plurality of buffers.

15. The method of claim 13, further comprising:

emptying the buffer of at least some of the data temporarily stored in the I/O controller to create a new amount of available memory credits in the I/O controller.

16. The method of claim 15, wherein emptying at least some of the data comprises:

sending the data to at least one I/O bus coupled to the I/O controller.

17. The method of claim 16, wherein sending the data to at least one I/O bus comprises:

sending the data to a plurality of I/O buses coupled to the I/O controller.

18. The method of claim 15, further comprising:

keeping track of the number of available memory credits in the I/O controller.

19. The method of claim 18, wherein keeping track of the number of memory credits comprises:

simultaneously keeping track of amounts of memory credits the I/O controller empties onto the I/O bus, amounts of memory credits sent to the I/O controller and amounts of memory credits made available by distribution of data sent from the chipset to a plurality of buffers contained within the I/O controller.

20. A system comprising:

a peripheral component interconnect (PCI) link;

a first input/output (I/O) bus;

a second I/O bus; and

an I/O controller coupled to the PCI link, the first I/O bus and the second I/O bus, the I/O controller comprising:

credit management logic to communicate to the PCI link an available amount of memory credits in the I/O controller,

a first buffer of a first memory size coupled to and in communication with the credit management logic, the PCI link and the first I/O bus, and

a second buffer of a second memory size couple to and in communication with the credit management logic, the PCI link and the second I/O bus.

21. The system of claim 20, wherein the first buffer and the second buffer are the same size.

22. The system of claim 21, wherein the first buffer and the second buffer are about 64 bytes to about 64 kilobytes in size.

23. The apparatus of claim 20, wherein the first buffer and the second buffer are different sizes.

24. The apparatus of claim 23, wherein the first buffer and the second buffer are about 64 bytes to about 64 kilobytes in size.

25. A machine readable medium having instructions stored therein which when executed cause a machine to perform a set of operations comprising:

determining an amount of available memory credits in an input/output (I/O) controller;

communicating to a chipset coupled to the I/O controller the amount of available memory credits; and

sending an amount of data from the chipset to the I/O controller, the amount of data sent being one of equivalent to and less than the communicated available memory credit amount.

26. The machine readable medium of claim 25, wherein determining the available amount of memory credits comprises:

comparing an amount of available memory in each of a plurality of buffers contained within the I/O controller; and

determining a least amount of available memory in one of the plurality of buffers to create an amount of available memory in the I/O controller.

27. The machine read medium of claim 26, having further instructions stored therein which when executed cause a machine to perform a set of operations further comprising:

temporarily storing the data in at least one buffer contained within the I/O controller;

emptying the buffer of at least some of the data temporarily stored in the I/O controller onto an I/O bus coupled to the I/O controller to create a new amount of available memory credits in the I/O controller; and

simultaneously tracking amounts of memory credits the I/O controller empties onto the I/O bus, amounts of memory credits sent to the I/O controller from the chipset and amounts of memory credits made available by distribution of the data sent from the chipset to a plurality of buffers contained within the I/O controller.